Abstract of the Disclosure

A semiconductor memory device comprises a memory-cell array for storing data, a peripheral circuit for carrying out an operation to read out or write data from or into the memory-cell array, read clock generation circuits (111, 113 and 115) each used for generating a read clock signal to be supplied to the peripheral circuit in the operation to read out data from the memory-cell array, write clock generation circuits (112, 114 and 116) each used for generating a write clock signal to be supplied to the peripheral circuit in the operation to write data into the memory-cell array. Since the pulse widths of the clock signals in read and writes are adjusted individually, margin insufficiencies of the pulse widths can be evaluated and results of the evaluation can be fed back to a design phase for, among other purposes, correction of a layout.